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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/656,541 | 09/06/2000 | William F. Beausoleil | POU9-2000-0047-US1 | 9916 |

34313 7590 06/03/2004

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| SHARON, AYAL I | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2123 | 11 |

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/656,541 | BEAUSOLEIL ET AL. | |
| | Examiner | Art Unit | |
| | Ayal I Sharon | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Introduction*

1. Claims 1-6 of U.S. Application 09/656,541, originally filed on 09/06/2000 are presented for examination. Applicants have submitted a terminal disclaimer (paper #10, filed 3/22/04) to overcome the double patenting rejections of the previous Office Action (paper #8, filed 12/17/03). Applicants have also filed evidence to show common ownership of U.S. Patent 6,618,698, which was used in the 35 USC §103 rejections. The 35 USC §103 rejections have consequently been withdrawn as per 35 USC §103(c).
2. The Double Patenting rejections and 35 USC §103 rejections have been withdrawn. New art rejections have been applied.

### *Drawings*

3. The drawings are objected to because figures are hand drawn, and are not legible. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Interpretation*

4. The claimed invention is disclosed to be an improvement over U.S. Patent 5,551,013 "Multiprocessor for Hardware Emulation", issued to Beausoleil et al. (See Specification, p.4). This patent has the same assignee, and common co-inventors (Beausoleil and Ng) as the instant application.
5. The claimed improvement is directed toward a method for transferring data between processors and their SDRAM memory via a bus.

### *Claim Rejections - 35 USC § 103*

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The prior art used for these rejections is as follows:
8. Harriman et al., U.S. Patent 6,330,645. (Henceforth referred to as "**Harriman**").
9. Chang, Hong-Kai et al. "Array Allocation Taking Into Account SDRAM Characteristics". Proc. of the 2000 Asia South Pacific DAC. January, 2000. pp.497-502. (Henceforth referred to as "**Chang**").
10. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

**11. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harriman in view of Chang.**

12. Harriman teaches the following limitations of Claim 1:

Claim 1. In a software driven emulator comprised of a plurality of modules on printed circuit boards,
(Harriman, especially: col.1, lines 40-52.)

Harriman discloses that "system on a chip" integration avoids some bandwith issues, but "increases the significance of bandwidth issues for remaining buses, including for example, memory controller / memory bandwidth issues".

each of said modules including a processor chip and at least one SDRAM coupled to the processor chip,
(Harriman, especially: col.2, lines 3-7)

Harriman teaches that "In one embodiment, the multiple memory controllers are provided as part of a system on a chip having two or more CPU's (or other requesters) as well as multiple memory controllers (and other components) on a single chip."

a maintenance bus coupled to said SDRAM, and a memory controller coupled to said maintenance bus,
(Harriman, especially: Fig.2, Item 234, and col.4, lines 7-11)

Harriman teaches that "Although many different types and levels of integration can be used in connection with features of the present invention, it is anticipated that typically the SDRAM 214 will be on a separate chip and will communicate with at least the memory control unit 220 via one or more buses 234."

a method executing bulk data transfers to said SDRAM via said maintenance bus, including the steps of:
(Harriman, especially: col.6, lines 40-45)

Harriman teaches that "The controller of Fig.3 manages 32-byte burst access to external SDRAM for the five on-chip clients." Examiner interprets "burst" as corresponding to "bulk".

However, Harriman does not expressly teach the following limitations:

transferring data **to** said SDRAM via said maintenance bus on each clock cycle for a predetermined number of clock cycles in succession;

halting the transfer of data after said predetermined number of data transfers;

initiating a SDRAM refresh cycle after said halting step;

resuming said transferring step upon receipt of a done signal after said refresh cycle.

Chang, on the other hand, does teach those limitations, as follows:

transferring data **to** said SDRAM via said maintenance bus on each clock cycle for a predetermined number of clock cycles in succession;
(Chang, especially: p.2, col.2, para. 1)

Chang teaches that "Accesses can be pipelined and we can send commands for new accesses to the SDRAM without waiting for the completion of the current access."

halting the transfer of data after said predetermined number of data transfers;
(Chang, especially p.2, col.1, last paragraph – p.2, col.2, first paragraph)

Chang teaches that "Note that two consecutive BA [bank active] commands for different banks must be separated by at least 2 cycles. After an R [read] command is performed, data is ready 3 cycles later. After a BP [bank pre-charge] command is performed, the corresponding bank does not accept any new command for 2 cycles."

Examiner interprets the required pauses between commands to correspond to the claimed limitation of "halting" the transfer of data.

initiating a SDRAM refresh cycle after said halting step;
(Chang, especially p.2, col.1, last paragraph – p.2, col.2, first paragraph)

Examiner interprets the BP [bank pre-charge] command as corresponding to the SDRAM refresh cycle.

resuming said transferring step upon receipt of a done signal after said refresh cycle.
(Chang, especially p.2, col.1, last paragraph – p.2, col.2, first paragraph)

Examiner interprets that the BA [bank active] command, which sends row address, corresponds to the claimed "done signal"..

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Harriman with those of Chang, because Harriman expressly teaches the use of SDRAMs, while Chang teaches their characteristics.

13. Harriman teaches the following limitations of Claim 2:

Claim 1. In a software driven emulator comprised of a plurality of modules on printed circuit boards,
(Harriman, especially: col.1, lines 40-52.)

Harriman discloses that "system on a chip" integration avoids some bandwith issues, but "increases the significance of bandwidth issues for remaining buses, including for example, memory controller / memory bandwidth issues".

each of said modules including a processor chip and at least one SDRAM coupled to the processor chip,
(Harriman, especially: col.2, lines 3-7)

Harriman teaches that "In one embodiment, the multiple memory controllers are provided as part of a system on a chip having two or more CPU's (or other requesters) as well as multiple memory controllers (and other components) on a single chip."

a maintenance bus coupled to said SDRAM, and a memory controller coupled to said maintenance bus,
(Harriman, especially: Fig.2, Item 234, and col.4, lines 7-11)

Harriman teaches that "Although many different types and levels of integration can be used in connection with features of the present invention, it is anticipated that typically the SDRAM 214 will be on a separate chip and will communicate with at least the memory control unit 220 via one or more buses 234."

a method executing bulk data transfers to said SDRAM via said maintenance bus, including the steps of:
(Harriman, especially: col.6, lines 40-45)

Harriman teaches that "The controller of Fig.3 manages 32-byte burst access to external SDRAM for the five on-chip clients." Examiner interprets "burst" as corresponding to "bulk".

However, Harriman does not expressly teach the following limitations:

transferring data **to** said SDRAM via said maintenance bus on each clock cycle for a predetermined number of clock cycles in succession;

halting the transfer of data after said predetermined number of data transfers;

initiating a SDRAM refresh cycle after said halting step;

resuming said transferring step upon receipt of a done signal after said refresh cycle.

Chang, on the other hand, does teach those limitations, as follows:

transferring data **from** said SDRAM via said maintenance bus on each clock cycle for a predetermined number of clock cycles in succession;
(Chang, especially: p.2, col.2, para. 1)

Chang teaches that "Accesses can be pipelined and we can send commands for new accesses to the SDRAM without waiting for the completion of the current access."

halting the transfer of data after said predetermined number of data transfers;
(Chang, especially p.2, col.1, last paragraph – p.2, col.2, first paragraph)

Chang teaches that "Note that two consecutive BA [bank active] commands for different banks must be separated by at least 2 cycles. After an R [read] command is performed, data is ready 3 cycles later. After a BP [bank pre-charge] command is performed, the corresponding bank does not accept any new command for 2 cycles."

Examiner interprets the required pauses between commands to correspond to the claimed limitation of "halting" the transfer of data.

initiating a SDRAM refresh cycle after said halting step;
(Chang, especially p.2, col.1, last paragraph – p.2, col.2, first paragraph)

Examiner interprets the BP [bank pre-charge] command as corresponding to the SDRAM refresh cycle.

resuming said transferring step upon receipt

of a done signal after said refresh cycle.
(Chang, especially p.2, col.1, last paragraph – p.2, col.2, first paragraph)

Examiner interprets that the BA [bank active] command, which sends row address, corresponds to the claimed "done signal"..

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Harriman with those of Chang, because Harriman expressly teaches the use of SDRAMs, while Chang teaches their characteristics.

14. Harriman does not expressly teach the limitations of Claim 3. Chang, on the other hand, does teach these limitations:

Claim 3. A method of executing bulk transfers as in claim 1 including establishing a starting address for said bulk transfer in said memory controller and incrementing said starting address by one on each clock cycle.
(Chang, especially Section III.C "Motivational Example", and Figs. 2-3)

Chang teaches that the BA [bank active] command sends a row address and the R [read] command sends column address and a read write signal. Examiner interprets that these addresses correspond to the claimed "starting address." Moreover, Fig.2 shows the behavior of an SDRAM multiple bank controller (see Section III.C). Chang teaches (also in Section III.C) that the controller accesses the pages of a bank sequentially, and then sequentially accesses the pages of "another bank".

Examiner interprets, based on Fig.1(b), and Section III.B.(i) that the banks are also accessed sequentially.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Harriman with those of Chang,

because Harriman expressly teaches the use of SDRAMs, while Chang teaches their characteristics.

15. Harriman does not expressly teach the limitations of Claim 4. Chang, on the other hand, does teach these limitations:

Claim 4. A method of executing bulk transfers as in claim 2 including establishing a starting address for said bulk transfer in said memory controller and incrementing said starting address by one on each clock cycle.
(Chang, especially Section III.C "Motivational Example", and Figs. 2-3)

Chang teaches that the BA [bank active] command sends a row address and the R [read] command sends column address and a read write signal. Examiner interprets that these addresses correspond to the claimed "starting address." Moreover, Fig.2 shows the behavior of an SDRAM multiple bank controller (see Section III.C). Chang teaches (also in Section III.C) that the controller accesses the pages of a bank sequentially, and then sequentially accesses the pages of "another bank".

Examiner interprets, based on Fig.1(b), and Section III.B.(i) that the banks are also accessed sequentially.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Harriman with those of Chang, because Harriman expressly teaches the use of SDRAMs, while Chang teaches their characteristics.

16. Harriman does not expressly teach the limitations of Claim 5. Chang, on the other hand, does teach these limitations:

Claim 5. A method of executing bulk transfers as in claim 1 wherein a data word is transferred on each clock cycle.

(Chang, especially: p.2, col.2, para. 1; and also Section III.C "Motivational Example", and Figs. 2-3)

Chang teaches that "Accesses can be pipelined and we can send commands for new accesses to the SDRAM without waiting for the completion of the current access."

Chang also shows in Fig.2, bottom row, that Data 1, Data 2, Data 3, and Data 4 are accessed on consecutive cycles, while in the EDO DRAM shown in Fig.3, they are not.

Examiner interprets, based on Fig.2, that the accessed data is "transferred on each clock cycle" within the "predetermined number of clock cycles in succession" claimed in Claim 1.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Harriman with those of Chang, because Harriman expressly teaches the use of SDRAMs, while Chang teaches their characteristics.

17. Harriman does not expressly teach the limitations of Claim 6. Chang, on the other hand, does teach these limitations:

Claim 6. A method of executing bulk transfers as in claim 2 wherein a data word is transferred on each clock cycle.
(Chang, especially: p.2, col.2, para. 1; and also Section III.C "Motivational Example", and Figs. 2-3)

Chang teaches that "Accesses can be pipelined and we can send commands for new accesses to the SDRAM without waiting for the completion of the current access."

Chang also shows in Fig.2, bottom row, that Data 1, Data 2, Data 3, and Data 4 are accessed on consecutive cycles, while in the EDO DRAM shown in Fig.3, they are not.

Examiner interprets, based on Fig.2, that the accessed data is "transferred on each clock cycle" within the "predetermined number of clock cycles in succession" claimed in Claim 2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Harriman with those of Chang, because Harriman expressly teaches the use of SDRAMs, while Chang teaches their characteristics.

***Conclusion***

18. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

19. Kreeger, K. et al. "Hybrid Volume and Polygon Rendering with Cube Hardware". Proc. of ACM SIGGRAPH/EUROGRAPHICS. 1999. pp.15-24.

20. Hobson, R. et al. "A Parallel Embedded-Processor Architecture for ATM Reassembly". IEEE/ACM Transactions on Networking. 1999. pp.23-37.

21. Kreeger (p.19) teaches the following:

> SDRAM provides information synchronized to the pipeline clock and provides burst mode access to obtain the maximum bandwidth possible if the memory can be organized correctly. Commonly available chips today typically utilize 4 internal banks which must be accessed in succession with bursts of at least 8 words per burst to be able to saturate the bandwidth between the chip and the memory controller.

> We propose to utilize memory chips with a word size of 16 bits. Therefore, four words must be read by each pipeline on each cycle and two words must be written. This means we would need six 16-bit memory interfaces per pipeline. An emerging technology in SDRAM chips is that of double data rate (DDR) which reads/writes data at both the rising and falling edges of the clock. Using DDR SDRAMS we can utilize two 16-bit memory interfaces for reading 64 bits per clock and one 16-bit memory interface for writing 32 bits per clock for a total of three 16-bit memory interfaces per pipeline.

22. Hobson (p.27) teaches the following:

> SDRAMs have a startup latency of several clock cycles. Thereafter, a new data word can be fetched/stored on every clock cycle.

***Correspondence Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

The fax phone numbers for the organization where this application or proceeding is assigned are:

All communications: (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Art Unit 2123

May 27, 2004